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10/751,096	12/31/2003	Jason Lin	SNDK.345US0	1337

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EXAMINER	
FARROKH, HASHEM	
ART UNIT	**PAPER NUMBER**
2187	

DATE MAILED: 03/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/751,096	LIN ET AL.	
	Examiner	Art Unit	
	Hashem Farrokh	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *16,18-26 and 30-32* is/are allowed.

6)☒ Claim(s) *1-4,6,8-15,17 and 27-29* is/are rejected.

7)☒ Claim(s) *5 and 7* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5/24/,4/28,613/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

The instant application having application No. 10/751,096 has a total of 32 claims pending in the application; there are 7 independent claims and 25 dependent claims, all of which are ready for examination by the examiner.

INFORMATION CONCERNING IDS:

The information disclosure statements (IDSs) submitted on 5/24/04, 4,28/05, and 6/13/05 was considered by the Examiner. The submissions are in compliance with the provisions of 37 CFR 1.97.

INFORMATION CONCERNING CLAIMS:

Claim Objections

1. Claims 5 is objected to because of the following informalities:

The expression "...he overhead..." in line 3 of claim 5 seems to be a typographical error.

Appropriate correction is required.

Claim Rejections

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> *The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.*

2. Claims 8 and 10 recites the limitation "said first flags" in line 1. There is insufficient antecedent basis for this limitation in the claim.

3. Claims 17, 27 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

4. Claim 17, line 3 recites: "second content is correctly programmed in the first data storage area", *this limitation is in conflict with the limitation in the parent claim 16, lines 6-7 which states*: "... programming second content including user data into a second data storage area..."

A clarification is required.

5. Claim 27, line 6 states: "...block is correctly successfully into the overhead..."; *there are two problems with this limitation that must be resolved:*

a) A term (e.g., erased) after successfully is missing

b) The expression "correctly successfully" *seems redundant, since either correctly or successfully would convey the intended meaning.*

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> *A person shall be entitled to a patent unless –*
>
> *(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.*

Claims 1-4, 9-10, 13-15, and 27-28 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent Publication No. 2002/0069314 A1 to Miyauchi et al. (hereinafter Miyauchi).

6. *In regard to claim 1 Miyauchi teaches:*

"A non-volatile memory **(element 15 in Fig. 1)** comprising a plurality of data storage areas **(e.g. see abstract; paragraphs 28-29 in page 2; element 15 in Fig. 1; Fig. 2)**, each of the data storage areas containing:" Miyauchi *discloses that flash or non-volatile memory consists of erasable storage blocks, each block comprises a plurality of storage groups, and each group comprises a plurality of sectors.*

"a user data portion;" **(e.g., see paragraph 29 in page 2; element 23 in Fig. 2).** *The Data Storage Area represents the user data portion recited in the claim.*

"and an overhead data portion," **(e.g., see paragraph 29 in page 2; elements 21-22 in Fig. 2).** *The Management Data Area represents the overhead data portion recited in the claim.*

"wherein the overhead data portion of each data storage area contains a first flag for indicating that another one of the data storage areas is correctly written." **(e.g., see paragraphs 39-40 and Table 2 in page 3; Figs 7A-7B).** *For example the latest data flag (F3) has been set to "1" indicating that latest or new group containing new data and inherently there is another group that contains data (e.g., old data), see Table 2.*

7. *In regard to claim 2 Miyauchi teaches:*

"wherein the overhead data portion of each of said data storage areas further contains a second flag for indicating that the data storage area itself is correctly written." **(e.g., see paragraphs 39-40 and Table 2 in page 3; Figs 7A-7B).** *For example Group Use Status Flag in Old Group (Table 2) for each sector is being set to 0 when data is written.*

8. *In regard to claim 3 Miyauchi teaches:*

"wherein each of said data storage areas corresponds to a sector of data." **(e.g., see paragraph 10 and Table 1).**

9. *In regard to claim 4 Miyauchi teaches:*

"wherein the data storage areas are organized into a plurality of units of erase, and wherein the overhead data portion of a predetermined data storage unit in each of the units of erase further contains a third flag for indicating that the unit of erase to which the predetermined data storage unit belongs has had an erase operation completed." **(e.g., see paragraph 30 and Table 2).** *For example F1 represents the third flag that is set to "0" when erase is completed.*

10. *In regard to claim 9 Miyauchi teaches:*

"wherein said data storage areas are written according to a predetermined sequence and wherein said another one of the data storage areas is the preceding data storage area in the sequence." **(e.g., see paragraph 43 page 4).** *Miyauchi teaches that sectors are written successively that represents the writing in the predetermined sequence recited in the claim.*

11. In regard to claim 10 Miyauchi teaches:

"wherein said first flags and the content of the user data portions are protected by error correction code (ECC)." **(e.g., see ECC data in Table 2; step s123 in Fig. 7B).**

12. In regard to claim 13 Miyauchi teaches:

"A memory **(element 15 in Fig. 1)**, comprising: a non-volatile memory comprising a plurality of data storage areas;" **(e.g. see abstract; paragraphs 28-29 in page 2; element 15 in Fig. 1; Fig. 2)**

"and a controller for the reading and writing of data to the memory **(element 14 in Fig. 1)**, wherein during a sequential write process of data into two or more of said data storage areas **(paragraph 43 in page 4)**, for each data storage area subsequent to the first, an indication of the write of the preceding data storage area is written into the current data storage area as part of its write process." **(e.g., see paragraphs 39-40 and Table 2 in page 3; Figs 7A-7B).** *For example the latest data flag (F3) has been set to "1" indicating that latest or new group containing new data and inherently there is another or preceding group that contains data (e.g., old data), see Table 2.*

13. In regard to claim 14 Miyauchi teaches:

"wherein during the sequential write process **(paragraph 40 in page 3)**, for the last of the data storage areas in the sequential process **(paragraph 40 in page 3)**, an indication of the write of the last of the data storage areas is written into the last of the

data storage areas." **(e.g., see paragraphs 39-40 and Table 2 in page 3; Figs 7A-7B).** *For example data is written successively sector to sector and F3*

14. In regard to claim 15 Miyauchi teaches:

"wherein each of said data storage areas includes a data portion **(element 23 in Fig. 2)** and an overhead portion **(elements 21-22 in Fig. 2)**, and wherein said indications are written into the overhead portion." **(e.g., see paragraph 29 in page 2).**

15. In regard to claim 27 Miyauchi teaches:

"A method of operating a non-volatile memory (**Paragraph 24 in page 2)**, comprising: erasing the data content of a block of the non-volatile memory (**Paragraph 29 in page 2)**, wherein the block comprises a plurality of sectors each having an data portion and an overhead portion;" **(e.g., see Paragraph 29 in page 2).** *For example each erase block comprise of plurality of groups and each group contains a plurality of sectors.*

"verifying that the block is successfully erased;" **(e.g., see Paragraph 30 in page 2).** *For example after successful erasure of the group the erase enable flag F1 set to "0".*

"and writing an indication that the block is correctly successfully into the overhead portion of a designated one of the sectors." **(e.g., see Paragraph 30 in page 2).** *For example after successful erasure of the group the erase enable flag F1 set to "0".*

16. In regard to claim 28 Miyauchi teaches:

"wherein said indication comprises a flag." **(e.g., see Paragraph 30 in page 2).**

Claims 11-12 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent Publication No. 2002/0026566 A1 to Awada et al. (hereinafter Awada).

17. In regard to claim 11 Awada teaches:

"A non-volatile memory **(Paragraph 32 in page 3; Fig. 2)** comprising a plurality of data storage areas," **(e.g., see Paragraph 94 in page 6; Fig. 5).** *For example information storage areas represents the data storage areas recited in the claim.*

"each of the data storage areas containing: a user data portion;" **(e.g., see Paragraph 94 in page 6; Fig. 5).** *For example Information Storage Area represents the user data portion recited in the claim.*

"and an overhead data portion," **(e.g., see Paragraph 94 in page 6; Fig. 5).** *For example Control-Data Areas represents the overhead data portion recited in the claim.*

"wherein the data storage areas are organized into a plurality of units of erase **(e.g., see Paragraph 68 in page 5)**, and wherein the overhead data portion of a predetermined data storage unit in each of the units of erase further contains a flag for indicating that the unit of erase to which the predetermined data storage unit belongs has had an erase operation completed." **(e.g., see Paragraph 148 in page 8).**

18. In regard to claim 12 Awada teaches:

"wherein said flag is comprised of multiple bits." **(e.g., see Paragraph 18 in page 2).**

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> *(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.*

Claim 29 is rejected under 35 U.S.C. 103(a) as being unpatentable over Miyauchi in view of Awada.

19. In regard to claim 29 Miyauchi teaches all limitation included in claim 28 but does not expressly teach: "wherein said flag is comprised of multiple bits."

Awada teaches: "wherein said flag is comprised of multiple bits." **(e.g., see Paragraph 18 in page 2)** *for using multiple bits status flag for erasing the sector data.*

Disclosures by Miyauchi and Awada are analogous because both references teach methods of operating flash or non-volatile memory.

At the time of invention it would have been obvious to a person of ordinary skill in art to modify the semiconductor storage device taught by Miyauchi to include the multiple bits status erase flags taught by Awada.

The motivation for using the method as taught by paragraph 7, page 1 of Awada is to provide an efficient data-backup scheme which obviate the limitations existed in prior art (see paragraphs 4-6, page 1).

Therefore, it would have been obvious to combine teachings of Awada with Miyauchto obtain the invention as specified in the claim.

ALLOWABLE SUBJECT MATTER

Claims 8 and 17 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Claims 16, 18-26 and 30-32 are allowed

Claims 5-7 are objected to as being dependent upon rejected based claims, but would be allowable if rewritten in correct and independent form including all of the limitations of the base claim and any intervening claims.

1. *The primary reason for allowance of claims 5-7 in instant application is the combination with the inclusion of the following limitations:* **wherein the data storage areas are organized into a plurality of units of erase, and wherein each of said blocks further contains an additional data storage area for overhead data portion of which having said second flag and not having said first flag.**

2. *The primary reason for allowance of claim 8in instant application is the combination with the inclusion of the following limitations:* **wherein said first flags are each composed of multiple bits**

3. *The primary reason for allowance of claims 16-20 in instant application is the combination with the inclusion of the following limitations:* **concurrently with said programming second content, writing to the second data storage area an indication that the first data storage area is correctly programmed**

4. *The primary reason for allowance of claims 21-26 in instant application is the combination with the inclusion of the following limitations:* **finding a first sector not**

indicated to be correctly programmed based upon content of the subsequent sector; and based on the content of the first sector itself, determining if the first sector is correctly programmed.

5. The primary reason for allowance of claims 30-32 in instant application is the combination with the inclusion of the following limitations: **subsequently recording in the overhead portion of a second sector an indication that said altering the data content of at least a first sector is successfully completed**

: IMPORTANT NOTE :

I f the applicant should choose to rewrite the independent claims to include the limitations recited in either one of the claims, the applicant is encouraged to ***amend the title of the invention*** *such that it is descriptive of the invention as claimed as required be sec.* ***606.01*** *of the* ***MPEP****. Furthermore, the* ***summary of invention*** *and the* ***abstract*** *should be amended to bring them into harmony with the allowed claims as required by paragraph 2 of* ***sec. 1302.01*** *of the* ***MPEP****.*

As allowable subject matter has been indicated, applicant's response must either comply with all formal requirements or specifically traverse each requirement not compiled with. See ***37 C.F.R. § 1.111(b)*** *and* ***§ 707.07(a) of the M.P.E.P.***

Conclusion

The prior art made of record and not relied upon are as follows:

1. U. S. Patent No. 5,838,614 to Estakhri et al. describes identification and verification of a sector within a block of mass storage flash memory.

2. U. S. Patent No. 5,601,132 B2 to Nomura et al. describes non-volatile memory and method of writing data thereto.

3. U. S. Patent No. 6,564,307 B1 to Micka et al. describes method, system, and program for logically erasing data.

Any inquiry concerning this communication should be directed to Hashem Farrokh whose telephone number is (571) 272-4193. The examiner can normally be reached Monday-Friday from ***8:00 AM to 5:00 PM.***

If attempt to reach the above noted Examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Donald A Sparks, can be reached on (571) 272-4201. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published application may be obtained from either private PAIR or Public PAIR. Status information for unpublished application is available through Private PAIR only. For more information about PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBS) at 866-217-9197 (toll-free).

HP
HF

2006-03-6

DONALD SPARKS
SUPERVISORY PATENT EXAMINER